# ACADEMIC REGULATIONS & CURRICULUM

## M.Tech. (VLSI)

**Applicable to the students admitted from the Academic year 2019-2020**

# MAHARAJ VIJAYARAM GAJAPATHI RAJ COLLEGE OF ENGINEERING

## (Autonomous)

(Approved by AICTE, New Delhi, and permanently affiliated to JNTUK, Kakinada)
Re-Accredited by NBA, Re-accredidated by NAAC with 'A' Grade,
Listed u/s 2(f) & 12(B) of UGC Act 1956.
Vijayaram Nagar Campus, Chintalavalasa,
Vizianagaram-535005, Andhra Pradesh

# The visionaries

**Late Dr. P V G Raju**
Raja Saheb of Vizianagaram
Founder Chairman-MANSAS
Ex-Minister for Education and Health, Govt. of AP
Ex Member of Parliament

**Late Dr. P. Anand Gajapathi Raju**
**Ex-Chairman-MANSAS**
Ex-Minister for Education and Health
Govt. of AP
Ex Member of Parliament

**P. Ashok Gajapathi Raju**
**Chairman-MANSAS**
Ex-Union Minister for Civil Aviation,
Govt. of India
Ex-Minister for Finance, Govt. of AP

# Vision

Maharaj Vijayaram Gajapathi Raj College of Engineering strives to become a centre par excellence for technical education where aspiring students can be transformed into skilled and well-rounded professionals with strong understanding of fundamentals, a flair for responsible innovation in engineering practical solutions applying the fundamentals, and confidence and poise to meet the challenges in their chosen professional spheres.

## Mission

The management believes imparting quality education in an atmosphere that motivates learning as a social obligation which we owe to the students, their parents/guardians and society at large and hence the effort is to leave no stone unturned in providing the same with all sincerity. Towards that end, the management believes special focus has to be on the following areas:

M1: Have on-board staff with high quality experience and continuously updating themselves with latest research developments and sharing that knowledge with students.

M2: Having a well stream-lined teaching learning process that is continuously assessed for effectiveness and fine-tuned for improvement.

M3: Having state-of-the-art lab and general infrastructure that gives students the necessary tools and means to enhance their knowledge and understanding.

M4: Having a centralized department focused on improving placement opportunities for our students directly on campus and coordinating the training programs for students to Complement the curriculum and enhance their career opportunities.

M5: Having advanced research facilities and more importantly atmosphere to encourage students to pursue self-learning on advanced topics and conduct research.

**ABOUT THE INSTITUTION:**

Maharajah Alak Narayan Society of Arts and Science (MANSAS) is an Educational Trust founded by Dr. (late) P.V.G Raju, Raja Saheb of Vizianagaram in the hallowed memory of his father Maharajah Alak Narayan Gajapati with a view to confound socio-economic inequalities in the Vizianagaram principality executing a trust deed on 12-11-1958 duly established Maharajah's College and other educational institutions in and around Vizianagaram. The Trust is a charitable one published under Section 6 a (1) of A.P Charitable and Hindu Religious Institutions and Endowment Act 30 of 1987.

The object of the Trust is to manage the properties of educational institutions under it and to promote and advance the cause of education in general, besides awarding scholarships to deserving students enabling them to undergo special training in science and industries in and out of India. The Trust has made an uncompromising contribution to the nation by presenting the stalwarts.

Trust offers KG to PhD level education in Arts, Sciences, Law, Pharmacy, Humanities Education, Engineering and Management and presently houses 13 Educational Institutions. MVGR College of Engineering is one of the 13 Institutes.

**Other Institutions under MANSAS**

1. M.R. HIGH SCHOOL 1857
2. M.R COLLEGE **(NAAC ACCREDITED)** 1879
3. M.R. COLLEGE OF EDUCATION 1950
4. M.R. WOMENS COLLEGE **(NAAC ACCREDITED)** 1962
5. M.R. GIRLS HIGH SCHOOL 1974
6. M.R. MODEL HIGH SCHOOL 1974
7. M.R. ENGLISH MEDIUM SCHOOL 1979
8. M.R.V.R.G.R LAW COLLEGE 1987
9. M.R. P.G. COLLEGE **(NAAC ACCREDITED)** 1987
10. M.R.SCHOOL OF MANAGEMENT STUDIES 1994
11. M.R.V.R.G.R – II MEMORIAL JR. COLLEGE 1994
12. M.R. COLLEGE OF PHARMACY 2004

Maharaj Vijayaram Gajapathi Raj (MVGR) College of Engineering was established in the year 1997 by Maharaj Alak Narayan Society for Arts and Sciences (MANSAS) to impart quality technical education. The Institution is located in lush green, serene and pollution free environment spread over 60 acres of land in Chintalavalasa village situated in the outskirts of Vizianagaram, a fort city in the north coastal region of Andhra Pradesh.

**Institution at a glance:**

- MVGR is a 22 years old institution, established in 1997
- All eligible UG Programs (CHEMICAL, CIVIL, CSE, ECE, EEE, IT & MECHANICAL) were re-accredited by NBA.
- MBA program was also re-accredited by NBA.
- Had been re-accredited with Grade ‘A’ by NAAC of UGC
- Has Permanent affiliation with JN Technological University-Kakinada
- Listed under sections 2(f) & 12(b) of UGC act 1956.
- Approved by AICTE-New Delhi
- EIGHT departments are recognized as RESEARCH CENTERS by JNTU-K
- Granted Autonomy by UGC in 2015
- Campus of 60 acre

- Offering 7 UG and 5 M.Tech and MBA program
- About 250 faculty of which 84 Ph.D. Degree holders
- 83 Laboratories with an investment of about 13 crores
- Total built up area of about 7 Lakh sft
- About 42,000 volumes and Access to 8 international online journal packages like IEEE, SPRINGER, etc.
- 1420 Systems & 395 Mbps band width internet facility
- About Rs. 4 crore worth of on-going R&D projects
- Actively involved in civil engineering consultancy work as Third Party Quality Auditor for Vizianagaram Municipality
- WIPRO Recognized technology learning center and MISSION 10X partner institution
- Recognized National Instruments Academy for Training in LabView
- SIRO Recognition by DSIR
- Recognized PTC Centre of Excellence for Creo Training
- Identified by MSME as Business Incubation Centre
- APSSDC-Siemens Technical Skill Development Institute
- Recognized CMs SKILL EXCELLENCY CENTER (SEC)
- Micrsoft Ed-vantage Platinum Partner
- Institutional member of IUCEE
- Institutional Member of CII
- Member, Chamber of Commerce, Vizianagaram
- Green Campus award by Govt. of AP

MVGR College of Engineering is rated as one among the best engineering colleges in the state of Andhra Pradesh as it set up highest standards in all areas of curricular, co-curricular and extra-curricular activities and in students' placements. Based on industry and expert's feedback, the college is updating the curriculum from time to time. The college offers many value added add-on courses students and conducts training programs to meet the industries' requirements.

# Academic Regulations for M.Tech. Program

Applicable to the students admitted from the Academic year 2019-20 onwards.

## 1. PROGRAM STRUCTURE:

**M.TECH:**

| S.No | Category | Credits |
|---|---|---|
| 1 | Program core courses | 16 |
| 2 | Program Elective courses | 19 |
| 3 | Open Electives | 3 |
| 4 | Research Methodology and IPR | 2 |
| 5 | Mini Project with seminar | 2 |
| 6 | Dissertation / Industrial Project | 26 |
| 7 | Audit courses 2 | 0 |
| | Total | 68 |

**Open Elective**

1. Business Analytics
2. Composite Materials
3. Cost Management of Engineering Projects
4. Industrial Safety
5. Operations Research
6. Waste to Energy

**Audit course 1 & 2**

1. Constitution of India
2. Disaster Management
3. English for Research Paper Writing
4. Pedagogy Studies
5. Personality Development through Life Enlightenment Skills.
6. Sanskrit for Technical Knowledge
7. Stress Management by Yoga
8. Value Education

## 2. PROGRAM PATTERN:

The program is for 2 academic years - 4 semesters.

## 3. AWARD OF DEGREE:

A student will be declared eligible for the award of degree if he/she fulfills the following academic regulations.

- A student shall be declared eligible for the award of the degree, if he/she pursues a course of study for not less than two academic years and not more than four academic years.

- A student shall register for **68** credits and secure all **68** credits.
- Students who fail to complete Two Years Course of study within Four years shall forfeit their seat and their admission stand cancelled.

## 4. CERTIFICATION PROGRAMS:

| S.No. | Dept | Name of the Program |
|---|---|---|
| 1 | MECH | Windchill 10.2 PDM by Adroitec Engineering Solutions Pvt. Ltd., Hyderabad |
| 2 | MECH | Creo 2.0 by PTC |
| 3 | MECH | Edgecam by Verosoft, UK |
| 4 | MECH | ANSYS Training and Certification by Mechanical Department |
| 5 | MECH | AUTOCAD Training and Certification by Mechanical Department |
| 6 | MECH | Catia by APSSDC-Dassault Systemes, CM's Center of Excellence |
| 7 | MECH | Delmia by APSSDC-Dassault Systemes, CM's Center of Excellence |
| 8 | MECH | Simulia by APSSDC-Dassault Systemes, CM's Center of Excellence |
| 9 | MECH | 2-Wheeler Automobile Certification by APSSDC-SIEMENS |
| 10 | MECH | 4-Wheeler Automobile Certification by APSSDC-SIEMENS |
| 11 | MECH | Welding Certification by APSSDC-SIEMENS |
| 12 | MECH | CNC Certification by APSSDC-SIEMENS |
| 13 | MECH | Commercial Electrical Certification by APSSDC-SIEMENS |
| 14 | MECH | Solid Edge Certification by APSSDC-SIEMENS |
| 15 | CHEM | Chemical Process Design and Simulation by Simtech Simulations, Hyderabad |
| 16 | ECE | Embedded Systems by ThinkLABS, Mumbai |
| 17 | ECE | Labview by National Instruments Systems India Pvt. Ltd. |
| 18 | ECE | Unified Technology Learning Program (UTLP) by Wipro Mission 10X |
| 19 | CSE, IT | PEGA by Virtusa Corporation |
| 20 | CSE, IT | Microsoft technologies by Microsoft Corp. |
| 21 | CSE, IT | Ethical Hacking by EC-Council Academia |
| 22 | CSE, IT | Java and C by Talent Sprint |
| 23 | CSE, IT | Network Analyst (CCNA) by Cisco Systems Inc |
| 24 | CSE, IT | Java Programming (OCJP) and DBMS by Oracle |
| 25 | EEE | PLC, Drives and Automation by Siemens |
| 26 | EEE | PLC by New Dawn Automation |
| 27 | EEE | Home Electrical Certification by APSSDC-SIEMENS |
| 28 | Civil | Remote Sensing and GIS by Indian Institute of Remote Sensing |

a) The Institution shall offer the certification programs by itself or in collaboration with industry/such other Institutions deemed to have specialized expertise in the proposed area of training.

b) Only students of the Institution shall be eligible to register on payment of prescribed fee.

c) However, subject to availability of resources and the demand the Institution may offer the program to external candidates meeting the pre-qualification requirements and in the order of the merit.

d) The duration of the course and design of the content shall be done by the respective departments of the Institution by themselves or in collaboration with industry/such other institutions deemed to have specialized expertise in the proposed area of training.

e) If the duration of the course is less than or equal to 40 hours, it can be completed in one semester, otherwise, it can suitably distributed over a number of semesters.

f) Mere enrolment/registration for the program shall not entitle any claim for award of certificate.

g) A candidate shall be deemed eligible for the award of the certificate if he/she

- Attends at least 75% of scheduled training sessions
- Complies to all the requirements of submission of the assignments, presentations, seminars, projects, etc., and also appears for periodic tests.
- Shall attain minimum levels of performance in tests as prescribed.
- Shall remit such fee as deemed fit for the certification
- A candidate registered and failed to meet the requirements shall be permitted to repeat the said training one another time after remitting 25% of the fee fixed for the program as re-registration fee.

If the student is absent for the periodic tests, the test shall be re-conducted on payment of 10% of fee.

## 5. COURSES OFFERED:

| Name of the Program | Degree |
|---|---|
| UG Programs (Engineering & Technology) | B.Tech (Civil)<br>B.Tech.(EEE)<br>B.Tech.(Mech.)<br>B.Tech.(ECE)<br>B.Tech.(CSE)<br>B.Tech.(CHEM)<br>B.Tech.(IT) |
| PG Programs (Engineering & Technology) | M.Tech.(Structural Engineering)<br>M.Tech. (Power Systems)<br>M.Tech.(PDM)<br>M.Tech.(VLSI)<br>M.Tech.(CN&IS) |
| Other PG Programs | MBA |
| Research Programs | Ph.D in Civil, EEE, MECH, ECE, CSE, CHEM, MBA and MATHS |

## 6. DISTRIBUTION AND WEIGHTAGE OF MARKS:

All Theory courses will have 5 units and assessed for 100 marks, of which, 40 marks for internal assessment and 60 marks for semester end external examination.

**Internal Assessment:**

- **Subjective tests – 30 Marks**
- **Assignments - 10 Marks**
    - Two subjective tests shall be conducted each for 30 Marks.
    - Each subjective test shall be conducted for 90 Minutes and have 3 questions each for 10 marks (No choice).
    - Average of the two subjective tests shall be considered as performance in internals.
    - Assignments shall be assessed for 10 marks.

### Semester End Assessment:

- Semester End examination is for 60 marks (180 min). Question paper contains 5 questions (one from each unit with internal choice). Each question carries 12 marks. A student shall answer all 5 questions.

**a) LABORATORY/PRACTICE:**

All Laboratory/Practice courses are assessed for 100 marks, of which, 40 marks for internal assessment and 60 marks for Semester End Examination.

**Internal assessment: (40 Marks)**

- Continuous assessment: :20 Marks
- Internal test: :20 Marks

**Semester End Assessment: (60 Marks)**

- Semester End Examination is for 60 marks (180 min) conducted and assessed by both external and internal examiners.
- Both internal and semester end examination shall include assessment of the student on
    - ❑ Knowledge of principles/concepts involved
    - ❑ Experimental design
    - ❑ Result interpretation and analysis
    - ❑ Experimental report

**b) DRAWING/DESIGN/ESTIMATION:**

These courses are assessed for 100 marks, of which, 40 marks for internal assessment and 60 marks for semester end examination.

- Continuous assessment for 20 marks for each unit finally averaged to 20 marks.
- Two internal assessment tests are conducted during the semester which shall be assessed for another 20 marks by taking the average.

**c) Research Methodology & IPR** shall be evaluated internally for 50 marks by PRC at the end of I semester

**d) Mini Project with Seminar** shall be evaluated internally for 50 marks by PRC in the II semester

**e)** For **audit course** a student is deemed to satisfy the minimum contact hours, as prescribed by the department and shall also comply with the requirements for submission of assignments/projects. A student shall also opt for MOOCs and submit the certificate after completion of the course.

**f) PROJECT EVALUATION**:

Duration is TWO semesters –Minimum of 40 weeks period is mandatory to submit.

- PRC includes HOD and two other senior faculties, one being the guide.
- To register for project work, a student shall complete all the course work requirements of I and II semesters.
- The progress of the work shall be periodically reviewed by PRC.
- The PRC shall authorize /approve change of guide/topic/title as deemed fit.
- A student shall submit Status Report in line with the recommended project calendar as approved by PRC.
- Student has to submit draft copy of thesis/dissertation to PRC, and also shall make an oral presentation. He/she shall publish the work in journal or international conference of repute and relevance.
- A student shall make 5 copies of PRC approved work and submit.
- Candidates who have successfully passed all theory and lab courses shall be eligible for submitting the thesis.
- The thesis shall be adjudicated by the internal & external examiners and Head of the department.
- Student shall be examined for his contributions, knowledge along with the quality of the work through presentations and Viva-voce.
- The assessment of work shall be done on the following lines:
  - **Project phase -I** which includes Problem definition, Literature survey, tool specific knowledge shall be evaluated internally for 100 marks by PRC at the end of III semester.

- **Project phase II** shall be evaluated for 300 marks at the end of IV semester. Out of 300 marks, 120 marks shall be evaluated internally by PRC and remaining 180 marks shall be evaluated externally by the internal and external examiner.

- The evaluation of Project phase II shall be made on the following aspects.
    - Experimental/methodology design
    - Result analysis and interpretations
    - Report writing
    - Presentation
    - Viva-voce

## 7. ATTENDANCE REGULATIONS:

- A student shall be eligible to appear for end semester examinations, if he or she acquires a minimum of 75% of attendance in aggregate of all the subjects (Theory & Lab.) for the semester.
- Condonation of shortage of attendance in aggregate up to 10% (65% and above and below 75%) in each semester may be granted by the college academic committee.
- Shortage of attendance below 65% in aggregate of all the subjects (Theory & Lab) for the semester shall not be condoned.
- Detained student shall seek re- admission for that semester when offered within 4 weeks from the date of commencement of class work.

## 8. MINIMUM ACADEMIC REQUIREMENTS:

- A student is deemed to have satisfied the minimum academic requirements for a course on securing at least 24 marks out of 60 marks at semester end examination and overall minimum of 50 marks out of 100 marks including internal assessment.

## 9. GRADING SYSTEM:

Semester Grade Point Average (SGPA) for the current semester which is calculated on the basis of grade points obtained in all courses, except audit courses and courses in which satisfactory or course continuation has been awarded,

$$SGPA = \Sigma \text{ (course credits earned x Grade points)} / \Sigma \text{ (Total course credits in the semester.}$$

**CGPA= Σ (course credits earned x Grade points) up to successfully completed semesters / Σ (Total course credits up to successfully completed semesters)**

The UGC recommends a 10-point grading system with the following letter grades as given below:

| | | |
|---|---|---|
| O | (Outstanding) | 10 |
| A+ | (Excellent) | 9 |
| A | (Very Good) | 8 |
| B+ | (Good) | 7 |
| B | (Above Average) | 6 |
| P | (Pass) | 5 |
| F | (Fail) | 0 |
| Ab | (Absent) | 0 |

- iii. A student obtaining Grade F shall be considered failed and will be required to reappear in the examination.

**Illustration of Computation of SGPA and CGPA and Format for Transcripts**

Computation of SGPA and CGPA

**Illustration for SGPA**

| Course | Credit | Grade Letter | Grade point | Credit Point (Credit x Grade) |
|---|---|---|---|---|
| Course 1 | 3 | A | 8 | 3 X 8 = 24 |
| Course 2 | 4 | B+ | 7 | 4 X 7 = 28 |
| Course 3 | 3 | B | 6 | 3 X 6 = 18 |
| Course 4 | 3 | O | 10 | 3 X 10= 30 |
| Course 5 | 3 | C | 5 | 3 X 5 = 15 |
| Course 6 | 4 | B | 6 | 4 X 6 = 24 |
| | **20** | | | **139** |

Thus, **SGPA** =139/20 = 6.95

**Illustration for CGPA**

| **Semester 1** | **Semester 2** | **Semester 3** | **Semester 4** |
|---|---|---|---|
| Credit : 18 | Credit : 18 | Credit : 16 | Credit : 16 |
| SGPA:7.9 | SGPA: 7.8 | SGPA: 7.6 | SGPA: 8.0 |

Thus, **CGPA** = 18 x 7.9 + 18 x 7.8 + 16 x 7.6 + 16 x 8.0

$$\frac{142.2+140.4+121.6+128}{} = \mathbf{7.83}$$

## 10. ELIGIBILITY FOR AWARD OF DEGREE:

**M.Tech.:**

A student shall be eligible for award of the degree if he/she fulfills the following conditions:

1) Successfully completes all the courses prescribed for the Program.
2) CGPA greater than or equal to 5.5(Minimum requirement for Pass),

## 11. AWARD OF CLASS:

Eligible candidates for the award of M.Tech. Degree shall be placed in one of the following Classes based on CGPA.

| Class | CGPA |
|---|---|
| Distinction | $\geq 7.5$ |
| First Class | $\geq 6.5$ |
| Pass Class | $\geq 5.5$ |

## 12. INSTRUCTION DAYS

A semester shall have a minimum of 90 clear instruction days.

## 13. TRANSFERS FROM OTHER INSTITUTIONS SHALL NOT BE PERMITTED.

## 14. SUPPLEMENTARY EXAMINATIONS

Supplementary examinations shall be conducted along with regular examinations.

## 15. WITHHOLDING OF RESULTS

The result of a student shall be withheld

- If the student has not paid the dues, if any, to the institution.
- If any case of pending disciplinary action
- Involvement in any sort of malpractices etc.
- Involvement in ragging.

## 16. TRANSITORY REGULATIONS

A Candidate shall be readmitted from University regulations to A1 regulations or from A1 regulations to A2 regulations as per the guide lines of JNTUK.

## 17. AMENDMENTS TO REGULATIONS:

The Academic Council of MVGR College of Engineering (Autonomous) reserves the right to revise, amend, change or nullify the Regulations, Schemes of Examinations, and/ or Syllabi or any other such matter relating to the requirements of the program which are compatible to the contemporary/emerging trends effectively meeting the needs of society/industry/stake holding groups.

**18. Regulations for MALPRACTICES during the conduct of examinations**

| | Nature of Malpractices/Improper conduct | Punishment |
|---|---|---|
| 1 (a) | If the candidate possesses or keeps accessible in examination hall, any paper, note book, programmable calculators, Cell phones, pager, palm computers or any other form of material concerned with or related to the subject of the examination (theory or practical) in which he is appearing but has not made use of (material shall include any marks on the body of the candidate which can be used as an aid in the subject of the examination) | Expulsion from the examination hall and cancellation of the performance in that subject only. * |
| (b) | If the candidate gives assistance or guidance or receives it from any other candidate orally or by any other body language methods or communicates through cell phones with any candidate or persons in or outside the exam hall in respect of any matter. | Expulsion from the examination hall and cancellation of the performance in that subject only of all the candidates involved. In case of an outsider, he will be handed over to the police and a case is registered against him. * |
| 2 | If the candidate has copied in the examination hall from any paper, book, programmable calculators, palm computers or any other form of material relevant to the subject of the examination (theory or practical) in which the candidate is appearing. | Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted to appear for the remaining examinations of the subjects of that Semester/year. The Hall Ticket of the candidate is to be cancelled. * |
| 3 | If the candidate impersonates any other candidate in connection with the examination. | The candidate who has impersonated shall be expelled from examination hall. The candidate is also debarred and forfeits the seat. The performance of the original candidate, who has been impersonated, shall be cancelled in all the subjects of the examination (including practicals and project work) already appeared and shall not be allowed to appear for examinations of the remaining subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat. If the imposter is an |

| | | |
|---|---|---|
| | | outsider/candidate not on rolls, he will be handed over to the police and a case is registered against him. * |
| 4 | If the candidate mishandles the Answer book or additional sheet or takes out or arranges to send out the question paper during the examination or answer book or additional sheet, during or after the examination.<br>Also if the answer script is mutilated / damaged disturbing the shape, of the script, answers, the bar code intentionally. | Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester. He shall be debarred from class work and all examinations and be allowed to reregistered for the next subsequent odd or even semester only. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.* |
| 5. | Uses objectionable, abusive or offensive language in the answer paper or in letters to the examiners or writes to the examiner requesting him to award pass marks. | The same should be brought to the notice of CE who in turn in consultation with malpractice committee makes decision for cancellation of the performance in that subject.<br>* |
| 6. | Refuses to obey the orders of the Chief Superintendent/Assistant – Superintendent / any officer on duty or misbehaves or creates disturbance of any kind in and around the examination hall or organizes a walk out or instigates others to walk out, or threatens the officer-in charge or any person on duty in or outside the examination hall of any injury to his person or to any of his relations whether by words, either spoken or written or by signs or by visible representation, assaults the officer-in-charge, or any person on duty in or outside the examination hall or any of his relations, or indulges in any other act of misconduct or mischief which result in damage to or destruction of property in the examination hall or any part of the College campus or engages in any other act which in the opinion of the officer on duty amounts to use of unfair means or misconduct or has the tendency to disrupt the orderly conduct of the examination. | In case of students of the college, they shall be expelled from examination halls and cancellation of their performance in that subject and all other subjects the candidate(s) has (have) already appeared and shall not be permitted to appear for the remaining examinations of the subjects of that semester. The candidates also are debarred and forfeit their seats. In case of outsiders, they will be handed over to the police and a police case is registered against them.<br>* |
| 7. | Leaves the exam hall taking away answer script or intentionally tears of the script or any part thereof inside or outside the examination hall. | Expulsion from the examination hall and cancellation of performance in that subject and |

| | | |
|---|---|---|
| | | all the other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat. * |
| 8. | Possess any lethal weapon or firearm in the examination hall. | Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred and forfeits the seat. * |
| 9. | If student of the college, who is not a candidate for the particular examination or any person not connected with the college indulges in any malpractice or improper conduct mentioned in clause 6 to 8. | Student of the colleges expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester. The candidate is also debarred and forfeits the seat.<br>Person(s) who do not belong to the College will be handed over to police and, a police case will be registered against them. * |
| 10 | Comes in a drunken condition to the examination hall. | Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and |

| | | |
|---|---|---|
| | | project work and shall not be permitted for the remaining examinations of the subjects of that semester. * |
| 11 | Copying detected on the basis of internal evidence, such as, during valuation or during special scrutiny. | Cancellation of the performance in that subject and all other subjects the candidate has appeared including practical examinations and project work of that semester/year examinations.* |

*

**1. General :**

- Wherever the words "he", "him", "his", occur in the regulations, they include "she", "her", "hers".
- The academic regulation should be read as a whole for the purpose of any interpretation.
- In the case of any doubt or ambiguity in the interpretation of the above rules, the decision of the Vice-Chancellor is final.
- The University may change or amend the academic regulations or syllabi at any time and the changes or amendments made shall be applicable to all the students with effect from the dates notified by the University.

# Ragging

## Prohibition of ragging in educational institutions Act 26 of 1997

### Salient Features

- ⇨ **Ragging within or outside any educational institution is prohibited.**
- ⇨ **Ragging means doing an act which causes or is likely to cause Insult or Annoyance of Fear or Apprehension or Threat or Intimidation or outrage of modesty or Injury to a student**

| | Imprisonment upto | | Fine Upto |
|---|---|---|---|
| Teasing, Embarrassing and Humiliation | 6 Months | + | Rs. 1,000/- |
| Assaulting or Using Criminal force or Criminal intimidation |  1 Year | + | Rs. 2,000/- |
| Wrongfully restraining or confining or causing hurt |  2 Years | + | Rs. 5,000/- |
| Causing grievous hurt, kidnapping or Abducts or rape or committing unnatural offence |  5 Years | + | Rs. 10,000/- |
| Causing death or abetting suicide |  10 Months | + | Rs. 50,000/- |

**In Case of Emergency CALL TOLL FREE NO. : 1800 - 425 - 1288**

**LET US MAKE MVGR A RAGGING FREE CAMPUS**

# Ragging

## ABSOLUTELY NO TO RAGGING

1. **Ragging is prohibited as per Act 26 of A.P. Legislative Assembly, 1997.**
2. **Ragging entails heavy fines and/or imprisonment.**
3. **Ragging invokes suspension and dismissal from the College.**
4. **Outsiders are prohibited from entering the College and Hostel without permission.**
5. **Girl students must be in their hostel rooms by 7.00 p.m.**
6. **All the students must carry their Identity Cards and show them when demanded**
7. **The Principal and the Wardens may visit the Hostels and inspect the rooms any time.**

**PROGRAM STRUCTURE**
**M.TECH (VLSI)**

**Semester - I**

| S.No | Course Code | Course Title | Hours per week | | | Credits |
|---|---|---|---|---|---|---|
| | | | L | T | P | |
| **1** | A2VLT101 | RTL Simulation and Synthesis with PLD's | 3 | -- | -- | 3 |
| **2** | A2VLT102 | Digital IC Design | 3 | -- | -- | 3 |
| **3** | A2VLT2XX | Program Elective – I | 3 | -- | -- | 3 |
| **4** | A2VLT2XX | Program Elective - II | 3 | -- | -- | 3 |
| **5** | A2VLL101 | RTL Simulation and Synthesis Lab | -- | -- | 4 | 2 |
| **6** | A2VLL102 | CMOS Digital Design Lab | -- | -- | 4 | 2 |
| **7** | A2VLT105 | Research Methodology & IPR | 2 | -- | -- | 2 |
| **8** | A2ACA50_ | Audit Course - I | 2 | -- | -- | -- |
| | | | | | Total Credits | **18** |

**Semester - II**

| S.No | Course Code | Course Title | Hours per week | | | Credits |
|---|---|---|---|---|---|---|
| | | | L | T | P | |
| **1** | A2VLT103 | Analog IC Design | 3 | -- | -- | 3 |
| **2** | A2VLT104 | Partial Reconfigurable FPGA | 3 | -- | -- | 3 |
| **3** | A2VLT2XX | Program Elective - III | 3 | -- | -- | 3 |
| **4** | A2VLT2XX | Program Elective - IV | 3 | -- | -- | 3 |
| **5** | A2VLL103 | CMOS Analog Design Lab | -- | -- | 4 | 2 |
| **6** | A2VLL104 | Reconfigurable Computing Lab | -- | -- | 4 | 2 |
| **7** | A2VLP401 | Mini Project | -- | -- | 4 | 2 |
| **8** | A2ACA50_ | Audit Course - II | 2 | -- | -- | -- |
| | | | | | Total Credits | **18** |

**Semester – III**

| S.No | Course Code | Course Title | Hours per week | | | Credits |
|---|---|---|---|---|---|---|
| | | | L | T | P | |
| 1 | A2VLT2XX | Program Elective - V | 3 | -- | -- | 3 |
| 2 | A2OET3XX | Open Elective - I | 3 | -- | -- | 3 |
| 3 | A2VLP402 | Dissertation Phase – I | -- | -- | 20 | 10 |
| | | | | | Total Credits | **16** |

**Semester – IV**

| S.No | Course Code | Course Title | Hours per week | | | Credits |
|---|---|---|---|---|---|---|
| | | | L | T | P | |
| 1 | A2VLP403 | Dissertation Phase – II | -- | -- | 32 | 16 |
| | | | | | Total credits | 16 |

Program Elective - I

| | | |
|---|---|---|
| 1 | A2VLT201 | Memory Technologies |
| 2 | A2VLT202 | Digital System Design |
| 3 | A2VLT203 | MOS Device Modelling |

Program Elective – II

| | | |
|---|---|---|
| 1 | A2VLT204 | Full Custom Design |
| 2 | A2VLT205 | Selected Topics in Mathematics |
| 3 | A2VLT206 | System Modelling & Simulation |

Program Elective - III

| | | |
|---|---|---|
| 1 | A2VLT207 | Low power VLSI Design |
| 2 | A2VLT208 | CMOS Mixed Signal VLSI Design |
| 3 | A2VLT209 | VLSI Signal Processing |

Program Elective - IV

| | | |
|---|---|---|
| 1 | A2VLT210 | Testing and Testability |
| 2 | A2VLT211 | Optimization Techniques & Applications to VLSI |
| 3 | A2VLT212 | VLSI Physical Design Automation |

Program Elective - V

| | | |
|---|---|---|
| 1 | A2VLT213 | Communication Network |
| 2 | A2VLT214 | SoC Architecture |
| 3 | A2VLT215 | Scripting Languages |

Open Elective - I

| | | |
|---|---|---|
| 1 | A2OET301 | Business Analytics |
| 2 | A2OET302 | Composite Materials |
| 3 | A2OET303 | Cost Management of Engineering Projects |
| 4 | A2OET304 | Industrial Safety |
| 5 | A2OET305 | Operations Research |
| 6 | A2OET306 | Waste to Energy |

Audit Courses

| | | |
|---|---|---|
| 1 | A2ACA501 | Constitution of India |
| 2 | A2ACA502 | Disaster Management |
| 3 | A2ACA503 | English for Research Paper Writing |
| 4 | A2ACA504 | Pedagogy Studies |
| 5 | A2ACA505 | Personality Development through Life Enlightenment Skills |
| 6 | A2ACA506 | Sanskrit for Technical Knowledge |
| 7 | A2ACA507 | Stress Management by Yoga |
| 8 | A2ACA508 | Value Education |

| A2VLT101 | SEMESTER - I | L | T | P | C |
|---|---|---|---|---|---|
| | RTL SIMULATION AND SYNTHESIS WITH PLD's | 3 | - | - | 3 |
| | Total Contact Hours – 48 | | | | |

## SYLLABUS

**UNIT – I**

**Design Approaches :** Top down approach to design, Design of FSMs (Synchronous and asynchronous), Static Timing analysis, Meta-stability, Clock issues, Need and design strategies for multi-clock domain designs

**UNIT – II**

**Basics of Verilog HDL :** Verilog as HDL, Levels of Design Description, Module, Syntax and Semantics of Verilog; Basic Language Elements- Keywords, Identifiers, White Space, Characters, Comments, Numbers, Strings, Logic Values, Strengths, Data Types, Scalars and Vectors, Parameters, Operators, Modelling Techniques, System Tasks and Compiler Directives.

**UNIT – III**

**Programmable Devices :** Programmable Logic Devices, Introduction to ASIC Design Flow, FPGA elements- basic blocks, Programming Technologies- OTP, reprogrammable, I/O blocks, Programmable interconnects, Software , SoC, ESD protection.

**UNIT – IV**

**Field Programmable Gate Arrays:** Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable Interconnects, and Programmable I/O blocks in FPGAs, Dedicated Specialized Components of FPGAs and Applications of FPGAs.

**UNIT – V**

**IP And Prototyping :** IP in various forms: RTL Source code, Encrypted Source code, Soft IP, Net list, Physical IP, Use of external hard IP during prototyping. Case studies and Speed issues.

**TEXT BOOKS:**

1. Richard S. Sandige, Modern Digital Design, MGH, International Editions
2. Donald D Givone, Digital Principles and Design, TMH

**REFERENCE BOOKS:**

1. Field Programmable Gate Array Technology, Stephen M. Trimberger, Springer International Edition.
2. Samir Palnitkar, Verilog HDL, A Guide to Digital Design and Synthesis, Prentice Hall.

**COURSE OUTCOMES:**

CO1 : Students fully appreciate about the use of RTL in digital system design.
CO2 : Students gain the knowledge on Verilog HDL Coding.
CO3 : Students get an idea on Programmable Logic Devices design flow.
CO4 : Students fully appreciate about knowledge in FPGA's
CO5 : Students grasp the knowledge of IP's in prototyping.

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| Course designed by | Department of Electronics and Communication Engineering |
| Approval | Approved by: Meeting of Board of Studies held on 29-06-2019 |
| | Ratified by: 5th Meeting of Academic Counceil,13-07-2019 |

| A2VLT102 | SEMESTER - I | L | T | P | C |
|---|---|---|---|---|---|
| | DIGITAL IC DESIGN | 3 | - | - | 3 |
| | Total Contact Hours – 48 | | | | |

**SYLLABUS**

**UNIT – I**

**MOS Inverters Static and Switching Characteristics:** Resistive load inverter, Inverters with n-type MOSFET load, CMOS inverter, delay time definitions, Calculations of Delay Times, inverter design with delay constraints.

**UNIT – II**

**Combinational MOS Logic Circuits:** MOS logic circuits with depletion nmos loads, CMOS Logic Circuits, Complex Logic circuits, CMOS transmission gates (Pass Gates).

**UNIT – III**

**Sequential & Dynamic Logic Circuits:** Behavior of bistable elements, SR Latch Circuit, Clocked latch and flip-flop circuits, CMOS D-latch and edge triggered flip-flop, Basic principle of Pass transistor circuits, Voltage Boot strapping, Synchronous dynamic circuit techniques, Dynamic CMOS Circuit Techniques, High performance Dynamic CMOS circuits.

**UNIT – IV**

**Semiconductor Memories:** Introduction, MOS Decoders, Static RAM Cell Design, SRAM Column I/O Circuitry, Memory Architecture.

**UNIT – V**

**Additional Topics In Memory Design:** Introduction, Content-Addressable Memories (CAMs), Field Programmable Gate Array, Dynamic Read-Write Memories, Read-Only Memories, EPROMs, $E^2$PROMs, Flash Memory, FRAMs.

**TEXT BOOKS:**


1. CMOS Digital Integrated Circuits Analysis and Design, Sung-Mo Kang, TMH, Third Edition,, 2011.
2. Analysis and Design of Digital Integrated Circuits, David A. Hodges, Horace G. Jackson, and Resve A. Saleh, TMH, Third Edition, 2005.


**REFERENCE BOOKS:**


1. Digital Integrated Circuits, A Design Perspective, Jan M.Rabaey, Anantha Chandrakasan Borivoje Nikolic, Second Edition, PHI.
2. Digital Integrated Circuit Design, Ken Martin, Oxford University Press, 2011.


**COURSE OUTCOMES:**

CO1 : Students will be able to grasp the significance of MOS inverter static and switching characteristics.

CO2 : Student will be able to understand the combinational logic circuits.

CO3 : Students will be able to explain and analyze the sequential logic and dynamic logic circuits.

CO4 : Student will be able to grasp the significance of SRAM Read and Write Operations

CO5 : Student will be able to grasp the significance of DRAM, ROM, Flash Memory, FRAMs.

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| A2VLT201 | SEMESTER - I | L | T | P | C |
|---|---|---|---|---|---|
| | MEMORY TECHNOLOGIES | 3 | - | - | 3 |
| | Total Contact Hours – 48 | | | | |

## SYLLABUS

**UNIT – I**

**Random Access Memory Technologies (SRAM) :** SRAM Cell structures, MOS SRAM Architecture, MOS SRAM cell and peripheral circuit operation, Bipolar SRAM technologies, SOI technology, Advanced SRAM architectures and technologies, Application specific SRAMs.

**UNIT – II**

**Random Access Memory Technologies (DRAM) :** DRAM – DRAM technology development, CMOS DRAM, DRAM cell theory and advanced cell structures, BICMOS DRAM, soft error failure in DRAM, Advanced DRAM design and architecture, Application specific DRAM.

**UNIT – III**

**Non-Volatile Memories :** Masked ROMs, High density ROM, PROM, Bipolar ROM, CMOS PROMS, EPROM, Floating gate EPROM cell, One time programmable EPROM, EEPROM, EEPROM technology and architecture.
Non-volatile SRAM, Flash Memories (EPROM or EEPROM), advanced Flash memory architecture.

**UNIT – IV**

**Memory Fault Modeling Testing :** RAM fault modeling, Electrical testing, Pseudo Random testing, Megabit DRAM testing, non-volatile memory modeling and testing, IDDQ fault modeling and testing, Application specific memory testing.

**UNIT – V**

**Advanced Memory Technologies :** Introduction, Ferroelectric RAMs (FRAMs), Basic Theory, FRAM Cell and Memory operation, FRAM Technology Developments, FRAM Reliability Issues, FRAM Radiation Effects FRAM vs EEPROMs, GaAs FRAMs, Analog memories, magneto resistive RAMs (MRAMs), Experimental memory devices.

**TEXT BOOKS:**


1. Semiconductor Memories Technology – Ashok K. Sharma, 2002, Wiley.
2. Advanced Semiconductor Memories – Architecture, Design and Applications - Ashok K. Sharma- 2002, Wiley.


**REFERENCE BOOKS:**


1. Modern Semiconductor Devices for Integrated Circuits – Chenming C Hu, 1st Ed., Prentice Hall.
2. Digital Circuits Testing and Testability-P. K. Lala, Academic Press.

**COURSE OUTCOMES:**

CO1 : Students will fully appreciate about SRAM volatile memories in aspects of cell architectures, designs, technologies and applications.

CO2 : Students will fully appreciate about DRAM volatile memories in aspects of cell architectures, designs, technologies and applications.

CO3.: Students will fully appreciate about Non-Volatile memories in aspects of cell architectures, designs, technologies and applications.

CO4 : Students grasp the significance of fault modeling and testing of Volatile memory and Non-Volatile memory.

CO5 : Students will gain an Understanding of Advanced Memory Technologies.

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| Course designed by | Department of Electronics and Communication Engineering |
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| A2VLT202 | SEMESTER - I | L | T | P | C |
|---|---|---|---|---|---|
| | DIGITAL SYSTEM DESIGN | 3 | - | - | 3 |
| | Total Contact Hours – 48 | | | | |

## SYLLABUS

**UNIT– I**

**Minimization Procedures and CAMP Algorithm:** Review on minimization of switching functions using tabular methods, k-map, QM algorithm, CAMP-I algorithm, Phase-I: Determination of Adjacencies, DA, CSC, SSMs and EPCs, CAMP-I algorithm, Phase-II: Passport checking, CAMP-II algorithm: Determination of solution cube, Cube based operations, determination of selected cubes are wholly within the given switching function or not, Introduction to cube based algorithms.

**UNIT– II**

**PLA Design, PLA Minimization and Folding Algorithms:** Introduction to PLDs, basic configurations and advantages of PLDs, PLA- Introduction, Block diagram of PLA, size of PLA, PLA design aspects, PLA minimization algorithm (IISc algorithm), PLA folding algorithm (COMPACT algorithm) - Illustration of algorithms with suitable examples.

**UNIT– III**

**Design of Large Scale Digital Systems:** Algorithmic state machine charts-Introduction, Derivation of SM Charts, Realization of SM Chart, control implementation, control unit design, data processor design, ROM design, PAL design aspects, digital system design approaches using CPLDs, FPGAs and ASICs.

**UNIT– IV**

**Fault Diagnosis in Combinational Circuits:** Faults classes and models, fault diagnosis and testing, fault detection test, test generation, testing process, obtaining a minimal complete test set, circuit under test methods - Path sensitization method, Boolean difference method, properties of Boolean differences, Kohavi algorithm, faults in PLAs, DFT schemes, built in self-test.

**UNIT– V**

**Fault Diagnosis in Sequential Circuits:** Fault detection and location in sequential circuits, circuit test approach, initial state identification, Hamming experiments, synchronizing experiments, machine identification, distinguishing experiment, adaptive distinguishing experiments.

**TEXT BOOKS:**


1. Logic Design Theory, N.N.Biswas, PHI.
2. Switching and Finite Automata Theory, Z.Kohavi, 2nd Edition, 2001, TMH.


**REFERENCE BOOKS:**


1. Fundamentals of Logic Design, Charles H.Roth, 5th Ed, Cengage Learning.
2. Digital Design, Morris Mano, 3rd Edition, Prentice Hall.

**COURSE OUTCOMES:**

CO1 : Students will be able to appreciate the minimization techniques like k-map, QM method and CAMP Algorithm.

CO2 : Student will be able to grasp the significance of State diagrams, reliable ASM charts and design of sequential circuits using ROMs, PLAs, CPLD and FPGAs.

CO3 : Students will be able to minimize digital circuits through PLA minimization and Folding.

CO4 : Student will be able to design and analyze various Test Generation methods.

CO5 : Student will be able to gain an understanding of Fault Diagnosis in Sequential Circuits.

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| A2VLT203 | SEMESTER - I | L | T | P | C |
|---|---|---|---|---|---|
| | MOS DEVICE MODELING | 3 | - | - | 3 |
| | Total Contact Hours – 48 | | | | |

## SYLLABUS

**UNIT – I**

**Basic Device Physics:** Energy bands in solids, p-n Junctions, MOS Capacitors, Metal-Silicon Effect and High Field Effects.

**UNIT – II**

**MOSFET Devices:** Long Channel MOSFET, Short-Channel MOSFETS, MOSFET Scaling
**CMOS Devices Design:** MOSFET Scaling, Threshold Voltage, MOSFET Chanel Length.

**UNIT – III**

**CMOS Performance Factors:** Basic CMOS Circuit Elements, Parasitic Elements, Sensitivity of CMOS delay to device parameters, Performance Factors of Advanced CMOS Devices.

**UNIT – IV**

**Bipolar Devices:** NPN & PNP Transistors, Ideal Current-Voltage Characteristics, Bipolar Device Models for Circuit and Time-Dependent Analyses, Break down Voltages.
**Bipolar Device Design:** Design of Emitter Region, Design of Base Region, Design of Collector Region, Si-Ge based Bipolar Transistors, Modern Bipolar Transistor Structures.

**UNIT – V**

**Performance Factors:** Performance factors of CMOS, Performance factors of bipolar devices.

**TEXT BOOKS:**


1. Yuan Taur and T H Ning, Fundamentals of Modern VLSI Devices, 2nd Edition, Cambridge.
2. M.S. Tyagi, Introduction to Semiconductor Materials and Devices, Wiley, 2008.


**REFERENCE BOOKS:**


1. Ben G Streetman, Solid State Electronic Devices, 6th Edition, Pearson Prentice-Hall, 2009
2. Principals of CMOS VLSI Design, N.H.E Weste, K. Eshraghian, 2nd Edition, Addison Wesley.


**COURSE OUTCOMES:**

CO1: Grasp the knowledge about basic device physics.
CO2 : Grasp the knowledge about MOSFET devices.
CO3: Have the ability to understand and analyze CMOS Performance Factors.
CO4 : Grasp the knowledge on Bipolar devices and Bipolar device design.
CO5 : Have the ability to understand about performance factors of CMOS and Bipolar devices

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| A2VLT204 | SEMESTER - I | L | T | P | C |
|---|---|---|---|---|---|
| | FULL CUSTOM DESIGN | 3 | - | - | 3 |
| | Total Contact Hours – 48 | | | | |

## SYLLABUS

**UNIT – I**

Introduction, IC Design Flow, Schematic Fundamentals, Layout Design, Introduction To CMOS VLSI Manufacturing Processes, Layers And Connectivity, Introduction To Transistor Layout, Process Design Rules, Vertical Connection Diagram, A General Procedure To Layout Design.

**UNIT – II**

Significance of Full Custom IC Design, Layout Design Flows, Microprocessor Design Flow. An Application-Specific Standard Product (ASSP), Memories, System on a Chip, CAD Tools as Part of a Flow.

**UNIT – III**

Advanced Techniques For Specialized Building Blocks, Standard Cell Libraries, Special Logic Cells, Pad Cells, Memory Design Leaf Cells, Laser Fuse Cells And Chip Finishing Cells

**UNIT – IV**

Advanced Techniques For Building Blocks, Power Grid, Clock Signals And Interconnect Routing. Interconnect Layout Design, Special Electrical Requirements, Layout Design Techniques To Address Electrical Characteristics.

**UNIT – V**

Layout Considerations Due To Process Constraints: Wide Metal Slits, Large Metal Via Implementations, Step Coverage Rules, Multiple Rule Sets, Antenna Rules, Special Design Rules, Latch-Up And Guard Rings, Constructing The Pad Ring, Minimizing Stress Effects. Guidelines For Proper Layout, Proper Layout CAD Tools For Layout, Planning Tools, Layout Generation Tools, Support Tools.

**TEXT BOOKS:**


1. Dan Clein, CMOS IC Layout Concepts Methodologies and Tools, Newnes, 2000.
2. CMOS: Circuit Design, Layout, and Simulation by R. Jacob Baker


**REFERENCE BOOKS:**


1. Ray Alan Hastings, The Art of Analog Layout, 2nd Edition, Prentice Hall, 2006
2. IC Mask Design: Essential Layout Techniques by Christopher Saint and Judy Saint.
3. Design of Analog CMOS Integrated Circuit by B Razavi

**COURSE OUTCOMES:**

CO1: Students will grasp the knowledge on IC design flow.
CO2: Students will have the ability to grasp the knowledge about Layout design flow,
CO3: Students will be able to design different types of layout leaf cells.
CO4: Students will be able to apply layout design knowledge on specialized types of interconnect design.
CO5: Students will be able to apply the knowledge on efficient layout techniques to absorb process variations.

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| Course designed by | Department of Electronics and Communication Engineering |
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| A2VLT205 | SEMESTER - I | L | T | P | C |
|---|---|---|---|---|---|
| | Selected Topics in Mathematics | 3 | -- | -- | 3 |
| | Total Contact Hours – 48 | | | | |

## SYLLABUS

**UNIT – I**

**Probability and Statistics:** Definitions, conditional probability, Bayes Theorem and independence. Random Variables: Discrete, continuous and mixed random variables, probability mass, probability density and cumulative distribution functions, mathematical expectation, moments, moment generating function, Chebyshev inequality.

**UNIT – II**

**Special Distributions :** Discrete uniform, Binomial, Geometric, Poisson, Exponential, Gamma, Normal distributions, Pseudo random sequence generation with given distribution, Functions of a Random Variable

**UNIT – III**

**Joint Distributions :** Joint, marginal and conditional distributions, product moments, correlation, independence of random variables, bi-variate normal distribution.
Stochastic Processes: Definition and classification of stochastic processes, Poisson process, Norms, Statistical methods for ranking data.

**UNIT – IV**

**Multivariate Data Analysis :** Linear and non-linear models, Regression, Prediction and Estimation. Design of Experiments – factorial method, Response surface method

**UNIT – V**

**Graphs:** Basic terminology, multi graphs and weighted graphs, paths and circuits, shortest path Problems, Euler and Hamiltonian paths and circuits, factors of a graph, planar graph and Kuratowski's graph and theorem, independent sets, graph colouring.
**Trees:** Rooted trees, path length in rooted trees, binary search trees, spanning trees and cut set, theorems on spanning trees, cut sets , circuits, minimal spanning trees, Kruskal's and Prim's algorithms for minimal spanning tree.

**TEXT BOOKS:**


1. Henry Stark, John W. Woods, "Probability and Random Process with Applications to Signal Processing", Pearson Education, 3rd Edition.
2. C. L. Liu, "Elements of Discrete Mathematics", Tata McGraw-Hill, 2nd Edition.
3. Douglas C. Montgomery, E.A. Peck and G. G. Vining, "Introduction to Linear Regression Analysis", John Wiley and Sons, 2001.

**REFERENCE BOOKS:**


1. Douglas C. Montgomery, “Design and Analysis of Experiments”, John Wiley and Sons, 2001.
2. B. A. Ogunnaike, “Random Phenomena: Fundamentals of Probability and Statistics for Engineers”, CRC Press, 2010.


**COURSE OUTCOMES**

CO1 : Characterize and represent data collected from experiments using statistical methods.
CO2: Represent systems using the concepts of special distributions
CO3: Model physical process/systems with multiple variables towards parameter estimation and prediction
CO4: Perform trade studies across multiple dimensions while taking into account the effects of all variables on the responses of interest.
CO5: Represent systems/architectures using graphs and trees towards optimizing desired objective.

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| A2VLT206 | SEMESTER - I | L | T | P | C |
|---|---|---|---|---|---|
| | SYSTEM MODELING AND SIMULATION | 3 | - | - | 3 |
| | Total Contact Hours – 48 | | | | |

## SYLLABUS

**UNIT – I**

**Introduction :** Basic Simulation Modeling, Systems, Models and Simulation, Discrete Event Simulation, Simulation of single server queuing system, Simulation of Inventory System, Parallel/Distributed Simulation and the High level Architecture.

**UNIT – II**

**Simulation Software and Models:** Comparison of simulation packages with Programming languages, Classification of Simulation Software, Desirable Software features, General purpose simulation packages, Object Oriented Simulation, Examples of application oriented simulation packages. Guidelines for determining levels of model detail, Techniques for increasing model validity and credibility.

**UNIT – III**

**Time and Event Driven Models:** Modeling input signals, delays, System integration, Linear Systems, Motion control models, Numerical Experimentation, Simulation diagrams, Queuing theory, simulating queuing systems, and Types of Queues Multiple servers.

**UNIT – IV**

**Markov Process:** Disturbance signals, State Machines, Petri Nets & Analysis, System encapsulation, Probabilistic systems, Discrete Time Markov processes, Random walks, Poisson processes, the exponential distribution, simulating a poison process, and Continuous-Time Markov processes.

**UNIT – V**

**System Optimization:** System Identification, Searches, Alpha/beta trackers, Multidimensional Optimization, Modeling and Simulation methodology.

**TEXT BOOKS:**


1. System Modeling & Simulation, an Introduction, Frank L. Severance, John Wiley & Sons, 2001.
2. Simulation Modeling and Analysis. Averill M. Law, W. David Kelton, TMH, 3rd Edition, 2003.


**REFERENCE BOOKS:**


1. Systems Simulation, Geoffery Gordon, PHI, 1978.
2. System Modeling and Simulation, V. P. Singh, 1st Edition, New Age International.
3. Discrete-Event System Simulation, Jerry Banks , 5th Edition

**COURSE OUTCOMES:**

CO1: Students will grasp the knowledge on basic simulation modeling.
CO2: Students will have the ability to grasp the knowledge about software simulation models and their applications.
CO3: Students will be able to understand time and event driven models and simulations.
CO4: Students will grasp the knowledge on discrete and continuous time MARKOV process.
CO5: Students will be able to understand system optimization, modeling and simulation methodology.

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| Course designed by | Department of Electronics and Communication Engineering |
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| | Ratified by: 5th Meeting of Academic Counceil,13-07-2019 |

| A2VLT105 | SEMESTER - I | L | T | P | C |
|---|---|---|---|---|---|
| | Research Methodology and IPR | 2 | -- | -- | 2 |
| | Total Contact Hours – 30 | | | | |

**SYLLABUS**

**Unit – I**

Meaning of research problem, Sources of research problem, Criteria Characteristics of a good research problem, Errors in selecting a research problem, Scope and objectives of research problem. Approaches of investigation of solutions for research problem, data collection, analysis, interpretation, Necessary instrumentations

**Unit – II**

Effective literature studies approaches, analysis Plagiarism, Research ethics, Effective technical writing, how to write report, Paper Developing a Research Proposal, Format of research proposal, a presentation and assessment by a review committee

**Unit – III**

Nature of Intellectual Property: Patents, Designs, Trade and Copyright. Process of Patenting and Development: technological research, innovation, patenting, development. International Scenario: International cooperation on Intellectual Property. Procedure for grants of patents, Patenting under PCT.

**Unit – IV**

Patent Rights: Scope of Patent Rights. Licensing and transfer of technology. Patent information and databases. Geographical Indications.

**Unit – V**

New Developments in IPR: Administration of Patent System. New developments in IPR; IPR of Biological Systems, Computer Software etc. Traditional knowledge Case Studies, IPR and IITs.

**TEXT BOOKS :**


1. Stuart Melville and Wayne Goddard, "Research methodology: an introduction for science & engineering students'"
2. Wayne Goddard and Stuart Melville, "Research Methodology: An Introduction"
3. Ranjit Kumar, 2nd Edition, "Research Methodology: A Step by Step Guide for beginners"
4. Halbert, "Resisting Intellectual Property", Taylor & Francis Ltd ,2007.
5. Mayall, "Industrial Design", McGraw Hill, 1992.
6. Niebel, "Product Design", McGraw Hill, 1974.
7. Asimov, "Introduction to Design", Prentice Hall, 1962.
8. Robert P. Merges, Peter S. Menell, Mark A. Lemley, " Intellectual Property in New Technological Age", 2016.
9. T. Ramappa, "Intellectual Property Rights Under WTO", S. Chand, 2008

**COURSE OUTCOMES:**

CO1: Understand research problem formulation.

CO2: Analyze research related information and Follow research ethics

CO3: Understand that today's world is controlled by Computer, Information Technology, but tomorrow world will be ruled by ideas, concept, and creativity.

CO4: Understanding that when IPR would take such important place in growth of individuals & nation, it is needless to emphasis the need of information about Intellectual Property Right to be promoted among students in general & engineering in particular.

CO5: Understand that IPR protection provides an incentive to inventors for further research work and investment in R & D, which leads to creation of new and better products, and in turn brings about, economic growth and social benefits.

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| A2VLL101 | SEMESTER - I | L | T | P | C |
|---|---|---|---|---|---|
| | RTL SIMULATION AND SYNTHESIS LABORATORY | - | - | 4 | 2 |
| | Total Contact Hours – 48 | | | | |

- The students are required to design the logic circuit, test bench to perform the following experiments using necessary simulator (Xilinx Vivado Simulator/ Mentor Graphics Model sim Simulator) to verify the logical/functional operation and to perform the analysis with appropriate synthesizer (Xilinx ISE Synthesizer/ Mentor Graphics Precision RTL) and then validate the implemented logic with different hardware modules/kits (ZED board).
- The students are required to acquire the knowledge in both the Platforms (Xilinx Vivado and Mentor graphics) by perform at least TEN experiments.

## SYLLABUS

**List of Experiments:**

1. Realization of Logic Gates
2. SR,JK and T Flip Flop's
3. Priority Encoder
4. 8:1 Mux/Demux
5. 8-bit Magnitude comparator
6. Serial adder/ subtractor, parallel adder/subtractor, serial/parallel multiplier
7. Random Counter
8. Binary to Gray converter
9. Universal Shift Register
10. 4-bit Shift registers (SISO, SIPO, PISO, bidirectional)
11. 3-bit Synchronous Counters, Parity generator
12. Sequence generator/detectors, Synchronous FSM – Mealy and Moore machines

**Lab Requirements:**

**Software:**
Xilinx Vivado Suite, Precision RTL Synthesis, Model sim Simulator.

**Hardware:**
Personal Computer with necessary peripherals, configuration and operating system and relevant FPGA board hardware Kits.

**COURSE OUTCOMES:**

CO1 : Students fully appreciate about the use of Verilog HDL in digital system design.
CO2 : Students gain the knowledge on Xilinx Vivado Design suite.
CO3 : Students get an idea on design of digital circuits.
CO4 : Students get an exposure to Xilinx Vivado Synthesizer.
CO5 : Students grasp the knowledge of prototyping on FPGA board.

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| Course designed by | Department of Electronics and Communication Engineering |
| Approval | Approved by: Meeting of Board of Studies held on 29-06-2019 |
| | Ratified by: 5th Meeting of Academic Counceil,13-07-2019 |

| A2VLL102 | SEMESTER - I | L | T | P | C |
|---|---|---|---|---|---|
| | CMOS DIGITAL DESIGN LAB | - | - | 4 | 2 |
| | Total Contact Hours – 48 | | | | |

- The students are required to design and implement the Circuit and Layout of any TEN Experiments using CMOS 130nm Technology with Mentor Graphics Tool.

## SYLLABUS

**List of Experiments:**

1. Inverter Characteristics.
2. NAND and NOR Gate
3. XOR and XNOR Gate
4. 2:1 Multiplexer
5. Full Adder
6. RS-Latch
7. Clock Divider
8. JK-Master Slave Flip Flop
9. Synchronous Counter
10. Asynchronous Counter
11. Static RAM Cell
12. Dynamic Logic Circuit

**Lab Requirements:**

**Software:**

Mentor Graphics – Pyxis Schematic, IC Station, Calibre, ELDO Simulator

**Hardware:**

Personal Computer with necessary peripherals, configuration and operating System.

**COURSE OUTCOMES:**

CO1 : Students will be able to apply the knowledge of VLSI Design Methodologies using Mentor Graphics Tools.
CO2 : Student will be able to grasp the significance of various design logic Circuits in full-custom IC Design.
CO3 : Students will be able to apply the concepts of Physical Verification in Layout Extraction
CO4 : Student will be able to the design and analyze of CMOS Digital Circuits
CO5 : Student will be able to grasp the Significance of Pre-Layout Simulation and Post-Layout Simulation

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